

Notice of References Cited		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		09/982,061	MONROE, ERIC M.	
		Examiner	Art Unit	Page 1 of 2
		Akash Saxena	2128	

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*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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B	US-6,188,582	02-2001	Peter, Geoffrey	361/760
C	US-			
D	US-			
E	US-			
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J	US-			
K	US-			
L	US-			
M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages
U	"A Mechanism-Based Methodology for Processor Package Reliability Assessment", Nicholas P. Mencinger; Intel Technology Journal Q3, 2000; www.intel.com/technology/itj/q32000.htm
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W	"ReliaSoft's ALTA 1.0 - On Site Training Guide"; Realisoft Corporation; 1999; http://reliasoftware.com/
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